Roll No.

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Total Pages: 03

BT-3/D-22

43168

DIGITAL ELECTRONICS AND LOGIC DESIGN ES-217A

Time: Three Hours]

[Maximum Marks: 75

Note: Attempt Five questions in all, selecting at least one question from each Unit. All questions carry equal marks.

Unit I

1. (a) State and prove the De-Morgan theorem. Prove the following expressions:

$$\overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC} = \overline{AB} + \overline{BC} + \overline{CA}$$

 $(A + B)(C + D) = \overline{(\overline{A + B})(\overline{C + D})}.$

- (b) What are universal gates? Perform AND operation using NOR gate.
- (c) Reduce the following expressions using K-Map: $f = \Sigma$ (0, 1, 4, 5, 7, 13, 14, 15) + d (2, 9, 10, 12). Realise the obtained expressions using NAND/NOR logic.
- 2. (a) Explain the method of converting SOP representation into POS representation.

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	(b)	Perform the following operations in binary number
		system: 6
		(i) 23 + 15
		(ii) 16 - 36 (using 1's compliment)
		(iii) 17 - 9 (using 2's compliment).
	(c)	Design a four bit grey to binary and binary to grey
		code converter. 5
Unit II		
3.	(a)	Design a full adder using two half adders. 7
		What is Encoder? Design and explain the working
		of 8:3 encoder?
4.	Wha	t is Multiplexer? Explain working of 8: 1
	Mult	iplexer. How can 16: 1 MUX be designed using
	8:	1 Mux and OR gate ? Implement the function
	$f = \sum_{i=1}^{n} f_i$	E (1, 2, 6, 9, 13, 14, 15) using 8 : 1 Mux. 15
		Unit III
5.	(a)	Differentiate between latch and flip-flop. Explain
		the working of JK flip-flop. Explain race around
		condition of JK flip-flop. Also describe, how is it
		removed by master slave flip-flop?
	(b)	Convert D flip-flop to T flip-flop. 5
6.	(a)	Design mod 6 asynchronous counter. 7
	(b)	Design a bidirectional shift register. Explain its
		working. 8

Unit IV

- 7. (a) Mention specifications of DACs. Explain the working of weighted register D/A converter. 8
 - (b) Explain the working of flash type ADC. 7
- 8. (a) Explain the working of successive approximation type A/D converter.
 - (b) Differentiate between PAL and PLA. Implement NAND operation using PLA.

