Roll No. ..... Total Pages : 2

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BT-6/M-24

VERILOG HDL

Paper : EC-306A

Time : Three Hours] [Maximum Marks : 75

Note : Attempt *five* questions in all, selecting at least *one* question from each unit.

UNIT–I

1. (a) Discuss the conventional approach to digital design. 8

   (b) Explain scalars and vectors with illustrations. 7

2. (a) Write about "Module" in details. 8

   (b) List and explain various numbers used in Verilog HDL. 7

UNIT–II

3. (a) Using Gate level modelling, write and explain Verilog program for A-O-I gate circuit : 8

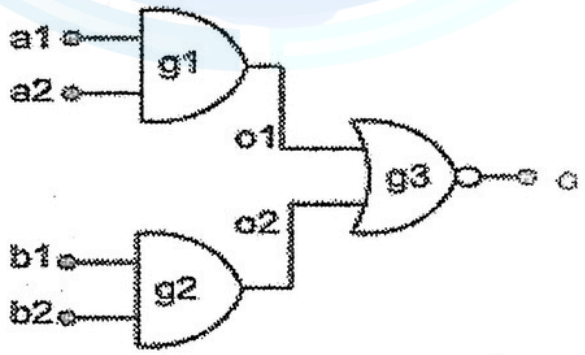

Fig 1: A-O-I gate circuit

(b) Explain functional bifurcation in details. 7

4. (a) Using Gate level modelling, write and explain Verilog program of 4 : 16 decoder. 8

(b) Explain case statement with an example. 7

UNIT–III

5. (a) Describe delays and continuous assignments in detail. 8

(b) List and explain various types of basic transistor switches. 7

6. (a) List and explain various types of operators used in Verilog HDL. 8

(b) Describe instantiations with strengths and delays. 7

UNIT–IV

7. (a) Explain the concept of functions with examples. 8

(b) Write a note on compiler directives. 7

8. (a) Explain the concept of tasks with examples. 8

(b) Write a note on hierarchical access. 7